



**XYALIS®**

**XYALIS**, an Electronic Design Automation (EDA) company, offers specialized tools in the area of Design for Manufacturing. XYALIS main tools includes CMP metal-fill and MCM and MPW layout optimization. These tools brings advanced solution to the most important DFM issues found during the design and the mask preparation. XYALIS tools also increase engineering productivity during tape-out and help reduce time to manufacturing.

Since 1995, a Chemical-Mechanical Polishing (CMP) step has been adopted in the semiconductor manufacturing process to flatten wafer surface between each metal layer. Metal density variations can badly impact this CMP process, thus the need for designers to insert "dummy tiles" into there design to help flatten the surface for each metal layer.

Since the beginning of the company, XYALIS has provided metal-fill tools to address this issue. The first member of this family has been GTiler. This tool has been in production use at major semiconductor site around the world for many years and has successfully completed a very high number of design tape-outs. It still provides the highest processing speed and the lowest database expansion factor.

In 2002 XYALIS introduced GTsmooth, a model-based CMP process estimator and dummy tiles insertion tool. The approach of inserting "dummy" metal tiles in all empty areas was not satisfactory because it introduced too many parasitics. Traditional methods were not successful in solving this problem and it was necessary to introduce a model based algorithm to get the best results and to minimize the number of inserted tiles while achieving the highest yield.

In 2006 XYALIS introduces GTstyle, a new tool for dummies insertion targeting 65nm processes and below. This new tool combines the advantages of the "model-based" approach while maintaining a compatibility with the design rules checks.

XYALIS is the only independent company offering a full line of products dedicated to the reticle assembly teams for wafer optimization and management.

The current toolset encompasses MPW optimization and placement plus the overall wafer frame management. XYALIS tools are very robust and has been used in production for more than 5 years at major semiconductor houses without any error.

XYALIS expertise and its success history are quite unique in the EDA industry. From the beginning, the company has focused on Design For Manufacturing tools and solutions to solve complex problems found between design and manufacturing. This area is now called DFM and is popular in the papers and symposiums. Thanks to its founders who have a very deep knowledge and experience in this field XYALIS has been able to innovate and provide new solutions to solve problems faced by engineers today.

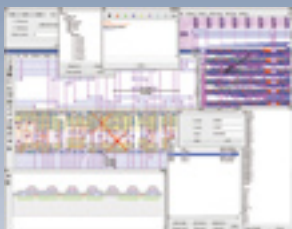
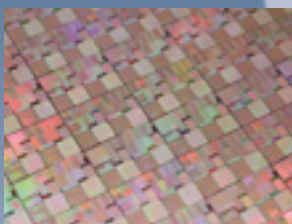
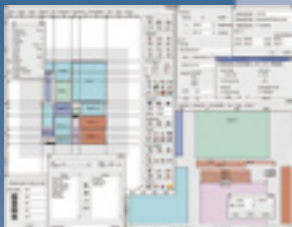
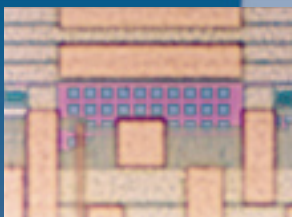
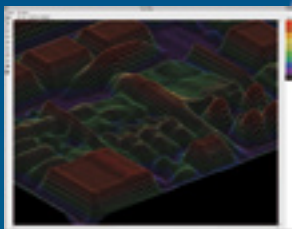
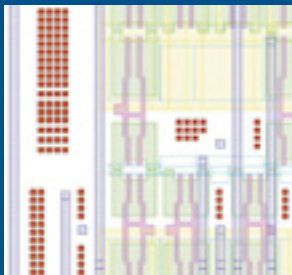
XYALIS is a privately held company, founded in 1998, with its headquarter in Grenoble, France.

XYALIS works closely with semiconductor industry leaders and can be found on the web at [www.xyalis.com](http://www.xyalis.com).

**Find out why 2 out of the top 3 semiconductor companies use Xyalis metal-fill solutions and why DRC solutions are inadequate. Call us today: tel. +33 476 706 475 E-mail: [info@xyalis.com](mailto:info@xyalis.com)**



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### **GTstyle**

#### **Hybrid metal filling tool**

GTstyle is the next generation of metal fill engine dedicated to the 65nm processes and below. It offers the power and efficiency of a model based approach with the simplicity of a rule based tool. Its unique features can accommodate complex metal fill rules while keeping a strict compatibility with DRC checks.

GTstyle usually generates between 50% and 85% less dummies than a pure rule based engine and by keeping dummies as far as possible from active geometries, it dramatically reduces parasitics and the impact on timing.

### **GTsmooth**

#### **Model based metal filling tool**

GTsmooth performs dummy tile insertion using a model based approach.

The model-based method identifies areas where dummies are needed to achieve maximum factory yield improvement. A rules-based method is used to insert tiles with respect to design rules and to keep computation time and database size very low. GTsmooth minimizes the number of inserted tiles to reduce induced parasitic effects. Typical dummies reduction with this tool can be as high as 95% versus the DRC methodology.

### **GTtiler**

#### **Rule based metal filling tool**

GTtiler is the fastest rules-based metal-fill tool for processes where a uniform density is mandatory to obtain the minimum thickness variation. GTtiler is simple to use and does not need a CMP model, it is very fast and generates a very small database.

With its unique engine specifically developed for dummies insertion, GTtiler offer advanced features not available with DRC tools like custom dummies shape, dummies stacking and grounding.

### **GTmuch**

#### **MPW assembly and job deck generation tool**

GTmuch is a complete environment for creating and editing the most complex Multi-Chip Modules (MCMs) and Multi-Project Wafers (MPWVs). GTmuch offers optimized assembly and placement capabilities specific to the need of MPW. GTmuch allows the Reticle Assembly team to maximize the wafer density and minimize the die size, while keeping the number of chips being impacted by sawing lines to a minimum.

### **GTframe**

#### **High performance frame generator tool**

GTframe is a frame editor that allows the insertion of items into an MPW (multi-project wafer) or an array of chips. These items can be tests dies, alignment marks or any GDSII files. GTframe is also able to insert any object into the scribe lines, between the chips of an MPW project or around the reticle (barcodes, titles...). GTframe unique scripting capabilities also allows the user to integrate the tool into its current flow and easily connect to other tools.

### **GTsuite**

#### **Complete suite of layout finishing tools**

GTsuite is a complete suite of layout finishing tools for common GDSII manipulation tasks like: GDSII checks, merge files, extract cells, replace cells, and remove layers.

With GTsuite, you are now able to process the GDSII databases of the largest designs, with the highest processing speed. By checking the consistency and integrity of multiple databases, GTsuite provides a safe transfer to silicon for the most complex SOC and MCM designs and must be included into every tape-out sign-off flow.



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