IC Layout finishing software

Advanced process dummy fill

UNIVERSALITY

Validated for production of digital processors down to 28nm as well as 1µ bipolar devices.

EFFICIENCY

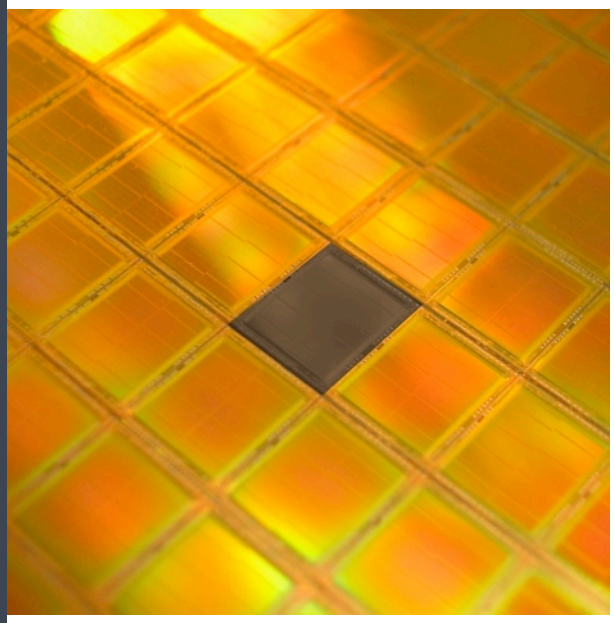
For the most demanding designs, GTstyle offers a parallel insertion mode, which splits the insertion algorithm onto different processors, dramatically speeding up the calculation and reducing memory usage.

RELIABILITY

XYALIS dummy filling engine has been used for years by leading edge IDM companies.

FLEXIBILITY

Dedicated to dummy fill, GTstyle provides advanced features to simplify setup for both process and design constraints.



- Advanced insertion algorithm
- Parasitic effect minimization
- Complex dummy tiles instantiation
- Tile interconnection
- Parallel insertion for maximum speed and minimum memory requirements

Deep sub-micron technologies require that process-related issues be taken into account during the design stage to achieve good manufacturing yield. To flatten the wafer surface between each metal layer, a Chemical-Mechanical Polishing (CMP) step is now implemented during the manufacturing process. Metal density variations badly impact the result of the CMP process, with non-uniform feature density causing CMP to over-polish empty areas and under-polish dense areas, and may result in functional and performance defects.

To increase manufacturing yield, designers must ensure a uniform pattern repartition over the chip and wafer. They insert “dummy tiles” into low-densities areas of their design, to help flatten the surface of each metal layer before CMP. These additional polygons, though electrically inactive, may cause parasitic effects that must be minimized and taken into account early in the design process in order to avoid any behavioral and timing issue.

XYALIS GTstyle is a dummy fill engine that has been used in production for the most challenging designs in the most advanced technology nodes. GTstyle maximizes CMP yield with a highly accurate patented tile insertion algorithm based on local density and roughness calculations and their variations over large areas.
GTstyle minimizes parasitic effects by limiting the number of tiles, by positioning them away from active geometries, and by balancing their instantiation around critical nets.
GTstyle’s parallel high-speed engine and its low memory consumption allow designers to integrate dummy tile insertion early in the design process.

XYALIS

BACKGROUND

GTstyle is XYALIS 3rd generation dummy fill engine, after a rule based tool and a model based tool. GTstyle provides all key features to meet both process and design requirements.

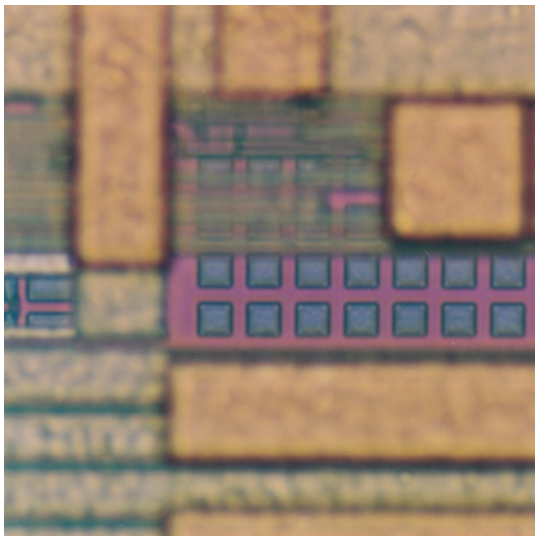
SYSTEM REQUIREMENTS

Software runs on any Linux workstation with RedHat 5 or above. Management of multi-cores or multi CPU is automatic.
A MacOSX version is also available. Binaries for other platforms may be provided upon request.

INFORMATION

For more information on any of our products or services please visit us on the Web at: **www.xyalis.com** or mail to: **sales@xyalis.com**

Features and Benefits



- **Advanced insertion algorithm**
  XYALIS GTstyle patented insertion algorithm combines global topology requirements with local design rules to instantiate dummy tiles. A unique topology analyzer calculates the local feature density over the chip, as well as the local roughness of the level, a critical parameter for copper technologies. An automatic gradient analyzer minimizes the local variations in density and roughness that negatively impact yield, taking into account scribe density at the chip border. This results in a minimum number of inserted tiles, up to 85% less than traditional rule-based dummy tile insertion algorithms, to meet the target density and roughness for the current technology.

- **Parasitic effect minimization**
  To minimize parasitics generated by tile insertion, designers can control the density of the inserted tiles and their positioning with regards to active geometries. The Keep Away function reduces parasitic capacitance by up to 90% by enforcing a minimum distance between dummy tiles and active geometries. Space around critical nets can be further increased to ensure timing specification conformance. And dummy tiles can be positioned along a non orthogonal insertion grid in order to enforce net balancing and avoid parasitics variations along the grid.

- **Complex dummy tiles instantiation**
  GTstyle inserts any type of dummy tiles, whatever their complexity: full-layers, regular tiles, post-OPC cells, diodes for grounding to bulk. To better control density over the different areas of the design, the insertion algorithm calculates the optimum tile size and merges dummy tiles into larger blocks if necessary.

- **Tile interconnection**
  GTstyle offers the possibility to replace floating capacitance of disconnected dummy tiles with an efficient shielding by inserting interconnection cells between contiguous dummy tiles. Interconnection cells may be defined horizontally and vertically, making it possible to stack dummy tiles through layers and to build dummy stripes within a layer.

- **Parallel processing for maximum speed**
  GTstyle high-speed one-pass algorithm and highly optimized output database, a few percents of the original layout database, allow dummy fill to run as often and early as necessary during design. Designers can take into account the impact of insertion on behavior and performance and avoid faulty tape-outs. A parallel insertion mode dramatically speeds up calculation and reduces memory size.

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